OIPE JC109 OCT 24 2003 PATENT & TRADEMARK OFFICE

PATENT
Intel/16406

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ju

Serial No.: 10/601,439

Filed: June 23, 2003

Assignee: Intel Corporation

For: Methods And Apparatus For Preserving Precise Exceptions In Code Reordering By Using Control Speculation

Group Art Unit: 2183

Examiner: Unknown

I hereby certify that this paper is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date:

October 21, 2003

James A. Flight
Registration No. 37,622
Attorney for Applicant

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The publications listed on the enclosed PTO Form-1449 are submitted pursuant to 37 CFR §§ 1.56, 1.97, and 1.98. Copies of the publications are enclosed.

TIME OF FILING

This information disclosure statement is being filed, to the best of the undersigned's knowledge, before the mailing date of a first Office action on the merits. In accordance with 37 CFR §1.97(b), no certification or fee is required.

METHOD OF PAYMENT

☒ No fee is required.

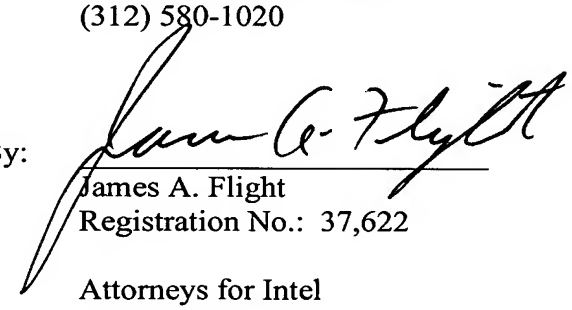
The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 50-2455. A copy of this paper is enclosed.

Correspondence Address:

Respectfully submitted,

GROSSMAN & FLIGHT, LLC.
20 N. Wacker Drive
Suite 4220
Chicago, Illinois 60606
(312) 580-1020

October 21, 2003

By: 

James A. Flight
Registration No.: 37,622

Attorneys for Intel

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Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. INTEL/16406	Serial No. 10/601,439
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant Ju	
		Filing Date **June 23, 2003**	Group Art Unit 2183

U.S. PATENT DOCUMENTS							
*EXAMINER INITIALS		DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS								
*Examiner Initials		Document Number	Publication Date	Country	Class	Subclass	Translation Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)		
	C01	Kemal Ebcioglu and Erik R. Altman, *Daisy: Dynamic Compilation for 100% Architectural Compatibility*, IBM Research Division (August 5, 1996).
	C02	Bich C. Le, *An Out-of-Order Execution Technique for Runtime Binary Translators*, Hewlett Packard Company (1998).
	C03	Erik M. Nystrom et al., *Code Reordering and Speculation Support for Dynamic Optimization Systems*, University of Illinois, Urbana-Champagne.

EXAMINER	DATE CONSIDERED
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not cinsidered. Include copy of this form with next communication to applicant.	